Amendments to Claims:

1. (original) A microcontroller with expandable memory banks, the microcontroller comprising:

a microprocessor;

a plurality of memory banks connected to the microprocessor for storing data, programs;

a memory bank control circuit connected to the microprocessor for asserting a signal during the processing of an interrupt event; and

a multiplexer for connecting the microprocessor with the plurality of memory banks, the multiplexer comprising:

a first input connected to an output of the microprocessor for bank switching during the normal operation;

a second input connected to a predetermined value corresponding to the memory bank storing the interrupt service routines; and

a selecting port connected to an output of the memory bank control circuit for selecting whether to output an page selection signal from the output of the microprocessor or an predetermined page selection signal, wherein the microprocessor can access data stored in the memory bank storing the interrupt service routines when the interrupt occurs.

2. (original) The microcontroller of claim 1 wherein the microprocessor is an MCS series microprocessor.

3. (original) The microcontroller of claim 1 wherein the plurality of memory banks are expandable and have a storage space larger than a command addressing capacity of the microcontroller.

4. (original) The microcontroller of claim 1 wherein the multiplexer further comprises extra input for a different predetermined page selection signal corresponding to the memory bank storing different interrupt service routines.

5. (original) The microcontroller of claim 1 wherein the memory bank control circuit generates a selection signal according to one of different interrupt sources.

6. (original) The microcontroller of claim 1 wherein each memory bank comprises a common area that does not comprise the interrupt service routines.

7. (original) The microcontroller of claim 1 wherein any program called by the interrupt service routine and the interrupt service routine are stored in the same memory bank.

8. (currently amended) A method for accessing a memory connected to a microprocessor, wherein the memory comprises a plurality of memory banks, the method comprising:

(a) storing interrupt service routines in only one of the plurality of memory banks;

(b) when an interrupt of the microprocessor does not occur, selecting and accessing a memory bank according to a page selection signal output by the microprocessor; and

(c) when an interrupt of the microprocessor occurs, immediately selecting and accessing the memory bank storing the interrupt service routines according to a predetermined page selection signal output by the microprocessor.

9. (original) The method of claim 8 wherein the microprocessor is an MCS series microprocessor.

10. (original) The method of claim 8 further comprises storing a common area not comprising the interrupt service routines in each memory bank.

11. (original) The method of claim 8 further comprises storing a program called by the interrupt service routines in the same memory bank with the interrupt service routines.

12. (new) A microcontroller with expandable memory banks, the microcontroller comprising:

a microprocessor for asserting a page selection signal, asserting a predetermined value corresponding to a memory bank storing an interrupt service routine, and asserting an interrupt signal when an interrupt occurs;

a plurality of memory banks coupled to the microprocessor for storing data and programs, and further for storing the interrupt service routine in only one of the memory banks;

a multiplexer coupled between the microprocessor and the plurality of memory banks for outputting a selection signal to the plurality of memory banks, the multiplexer comprising:

a first input coupled to the page selection signal for bank switching during normal operation;

a second input coupled to the predetermined value corresponding to the memory bank storing the interrupt service routine; and

a selecting port for switching between one of the page selection signal or the predetermined value to be outputted from the multiplexer as the selection signal; and

a memory bank control circuit coupled between the interrupt signal and the selecting port, the memory bank control circuit for controlling the multiplexer to select the predetermined value as the selection signal when the interrupt signal is asserted, and to select the page selection signal as the selection signal when the interrupt signal is not asserted;

wherein the plurality of memory banks is further for allowing the microprocessor to access a particular memory bank according to the selection signal.

13. (new) The microcontroller of claim 12 wherein the microprocessor is an MCS series microprocessor.

14. (new) The microcontroller of claim 12 wherein the plurality of memory banks are expandable and have a storage space larger than a command addressing capacity of the microcontroller.

15. (new) The microcontroller of claim 12 wherein the multiplexer further comprises an extra input for a different predetermined page selection signal corresponding to a memory

bank storing a different interrupt service routine.

16. (new) The microcontroller of claim 12 wherein the memory bank control circuit selects the selection signal according to one of different interrupt sources.

17. (new)) The microcontroller of claim 12 wherein each memory bank comprises a common area that does not comprise the interrupt service routine.

18. (new) The microcontroller of claim 12 wherein any program called by the interrupt service routine and the interrupt service routine are stored in the same memory bank.

19. (new) A method for accessing a plurality of memory banks, the method comprising:

providing a microprocessor for asserting a page selection signal, asserting a predetermined value corresponding to a memory bank storing an interrupt service routine, and asserting an interrupt signal when an interrupt occurs;

storing the interrupt service routine into only one of the memory banks;

selecting the predetermined value as a selection signal when the interrupt signal is asserted, and selecting the page selection signal as the selection signal when the interrupt signal is not asserted;

accessing a particular memory bank from the plurality of memory banks with the microprocessor according to the selection signal.

20. (new) The method of claim 8 wherein the microprocessor is an MCS series microprocessor.

21. (new) The method of claim 8 further comprising storing a common area not comprising the interrupt service routine in each memory bank.

22. (new) The method of claim 8 further comprising storing a program called by the interrupt service routine in the same memory bank as the interrupt service routine.